

Figure 1A

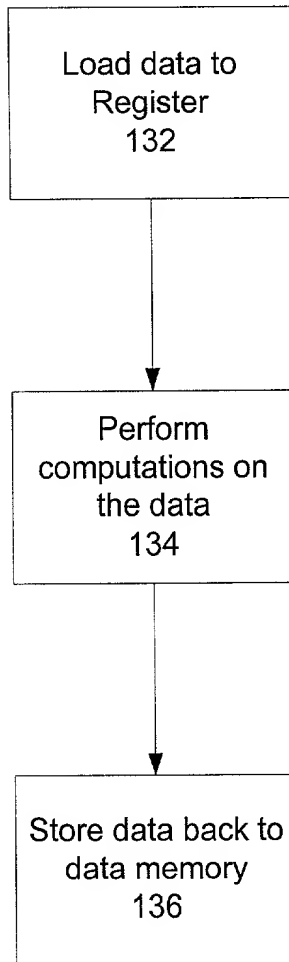


Figure 1B

OPCode 6 bits	Source1 Register 5 bits	Source2 Register 5 bits	Target Register 5 bits	Sub-OPCode 11 bits
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Figure 1C

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits
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Figure 1D

200

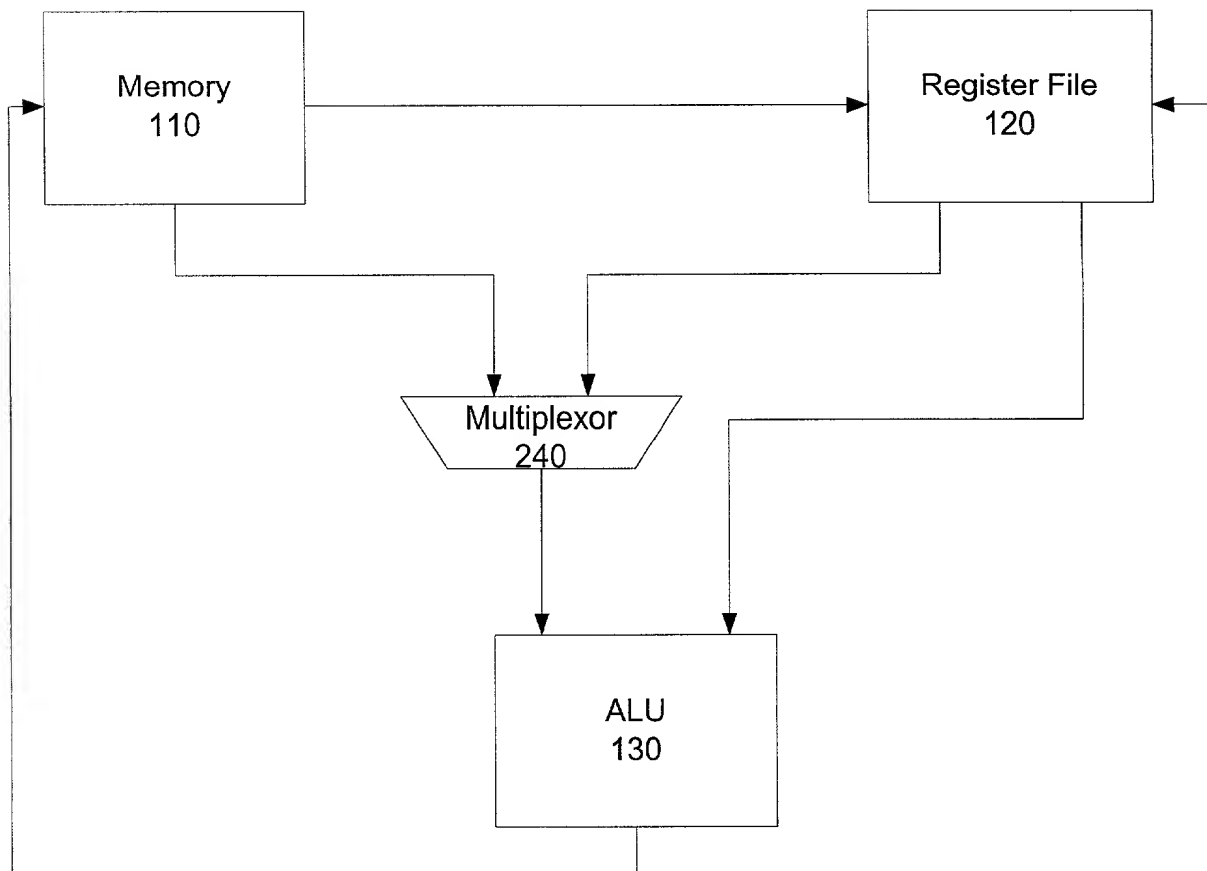


Figure 2

300

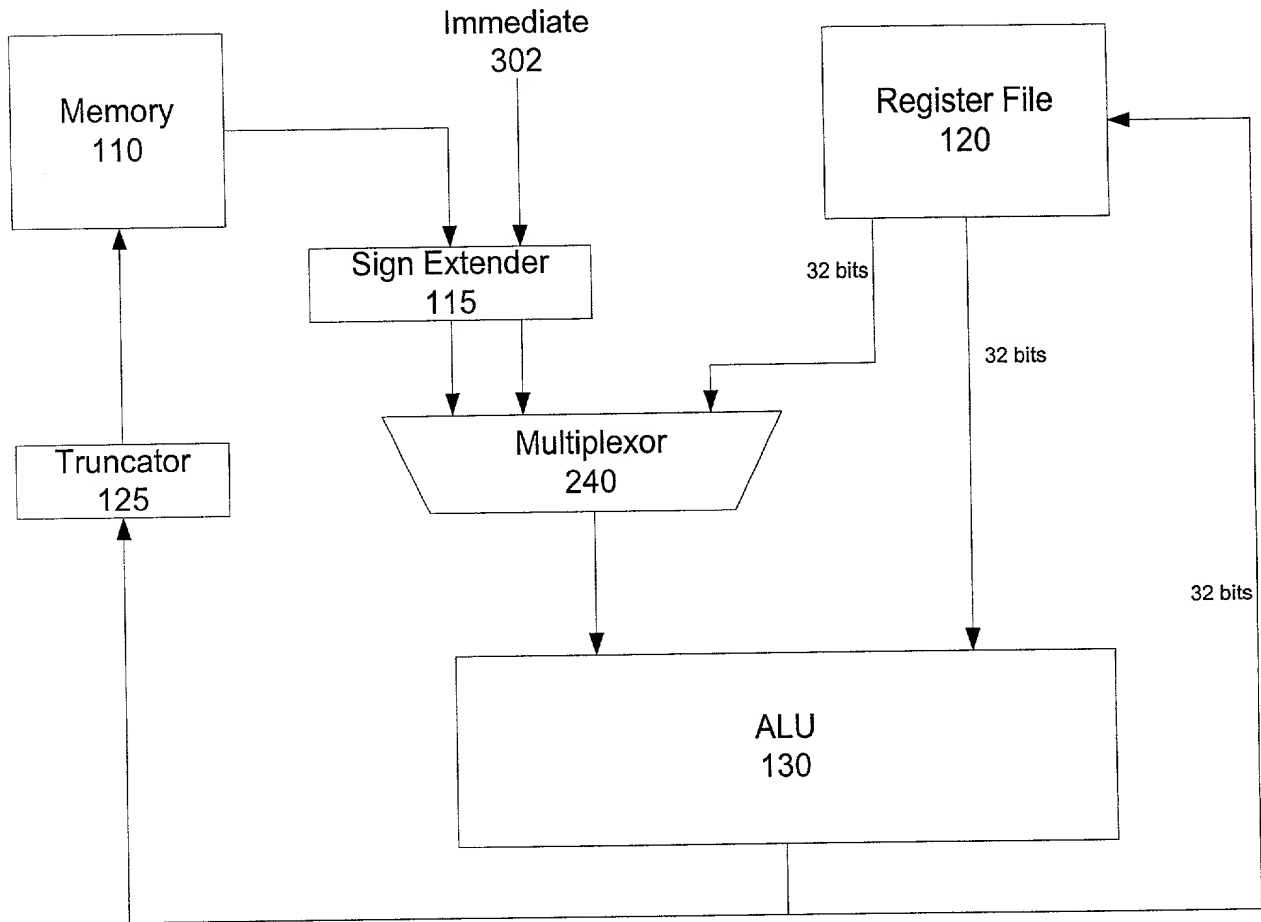


Figure 3A

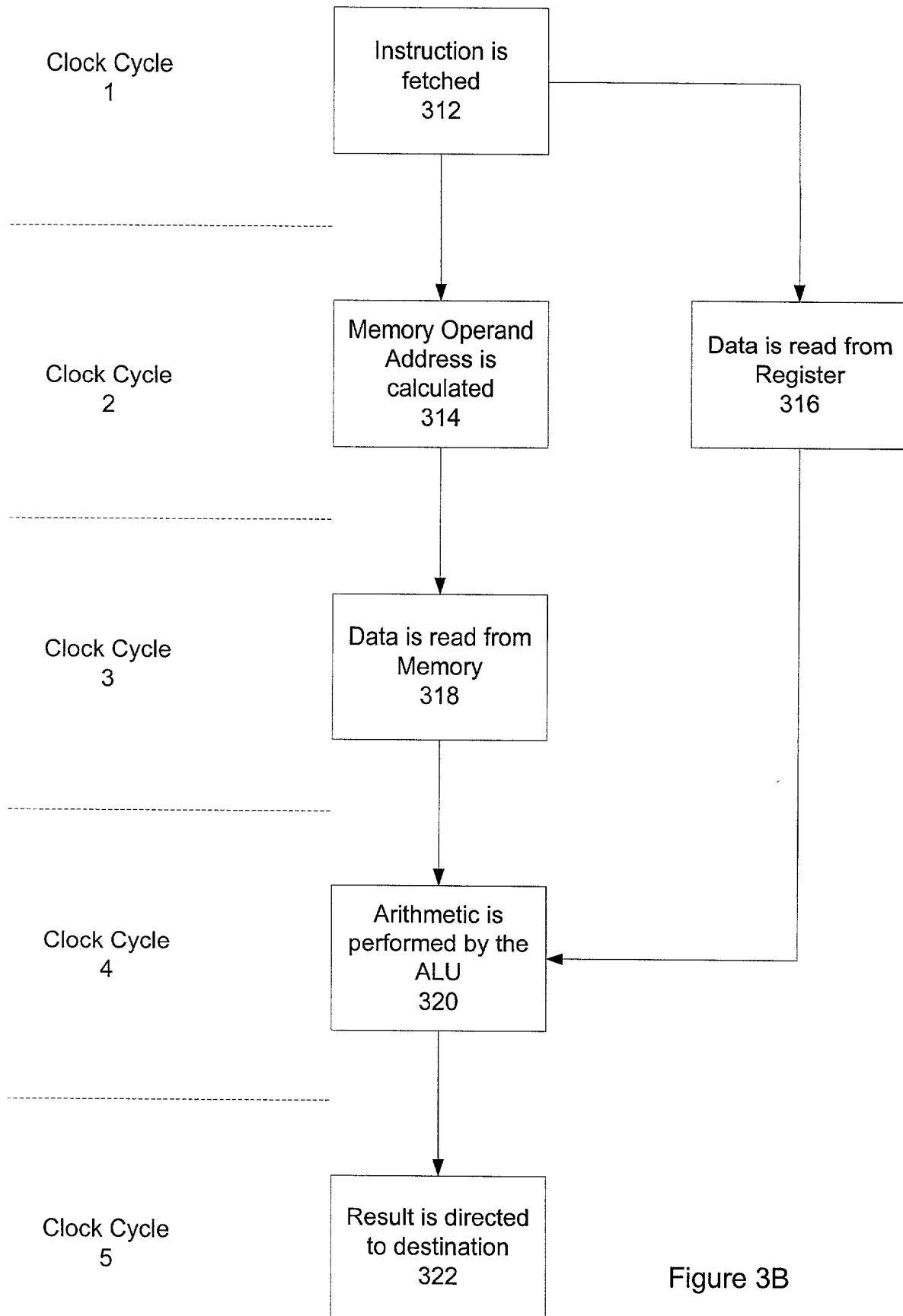


Figure 3B

400

OPCode 5 bits	Destination 11 bits	Source2 Register 5 bits	Source1 11 bits
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Figure 4

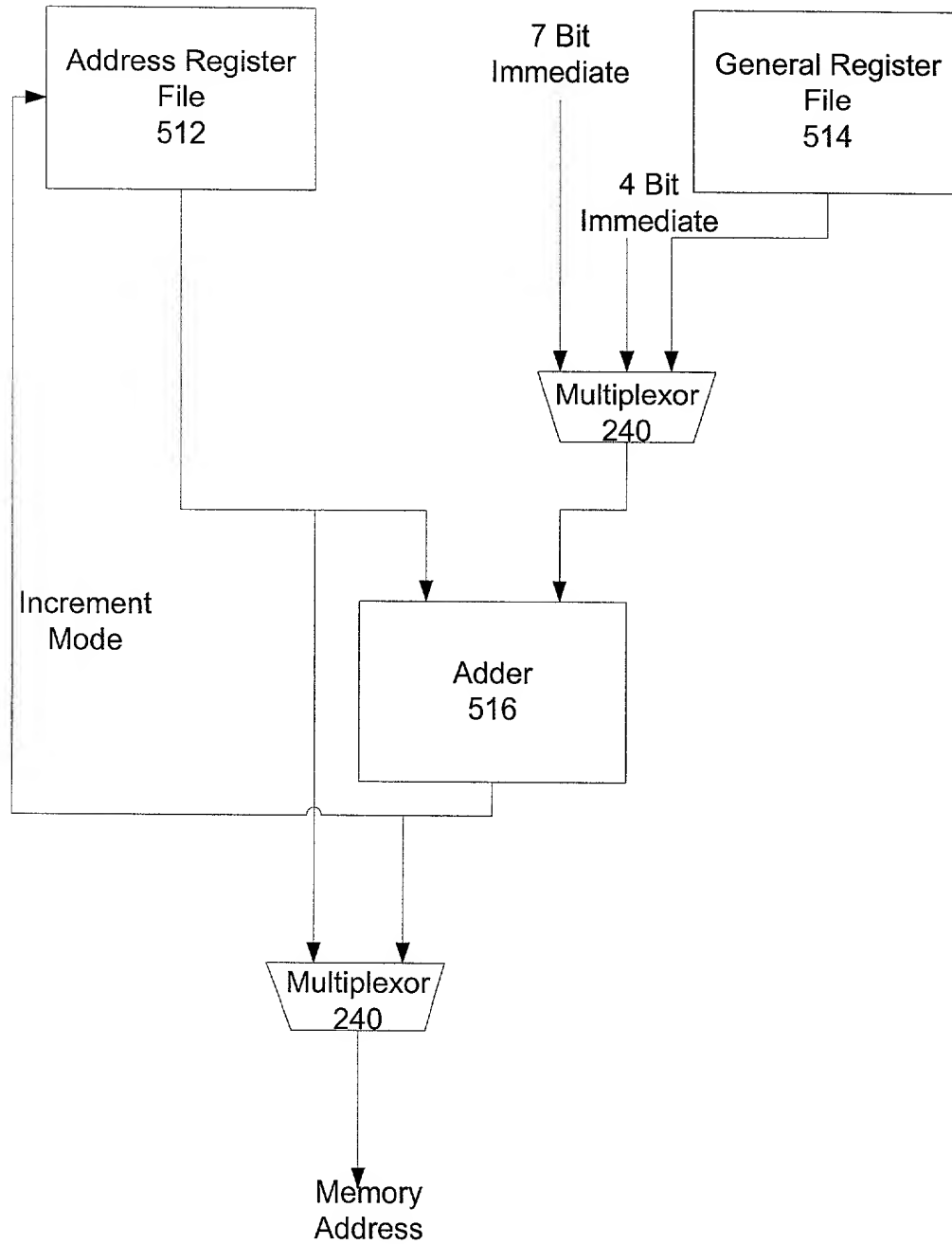


Figure 5

1	I ₆	I ₅	A ₂ A ₁ A ₀	I ₄	I ₃	I ₂	I ₁	I ₀	Row 1
0	1	1		R ₄	R ₃	R ₂	R ₁	R ₀	Row 2
0	1	0		M	I ₃	I ₂	I ₁	I ₀	Row 3
0	0	1	Register Direct						Row 4
0	0	0	Immediate						Row 5

Figure 6

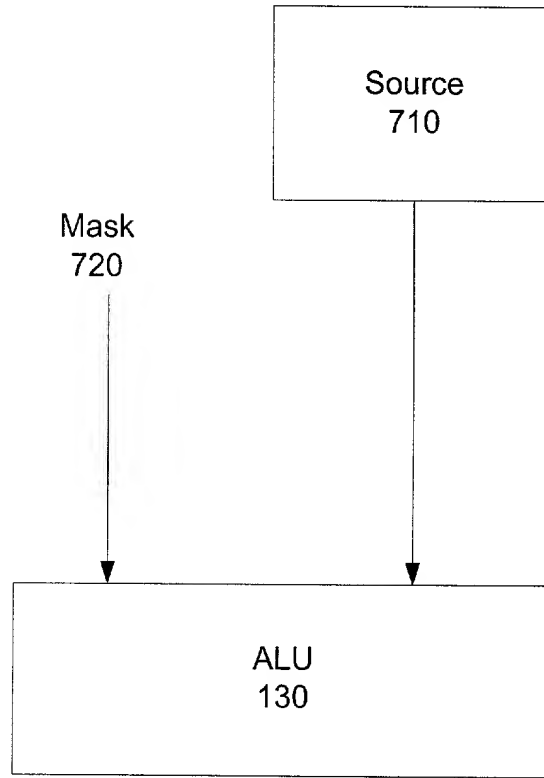


Figure 7

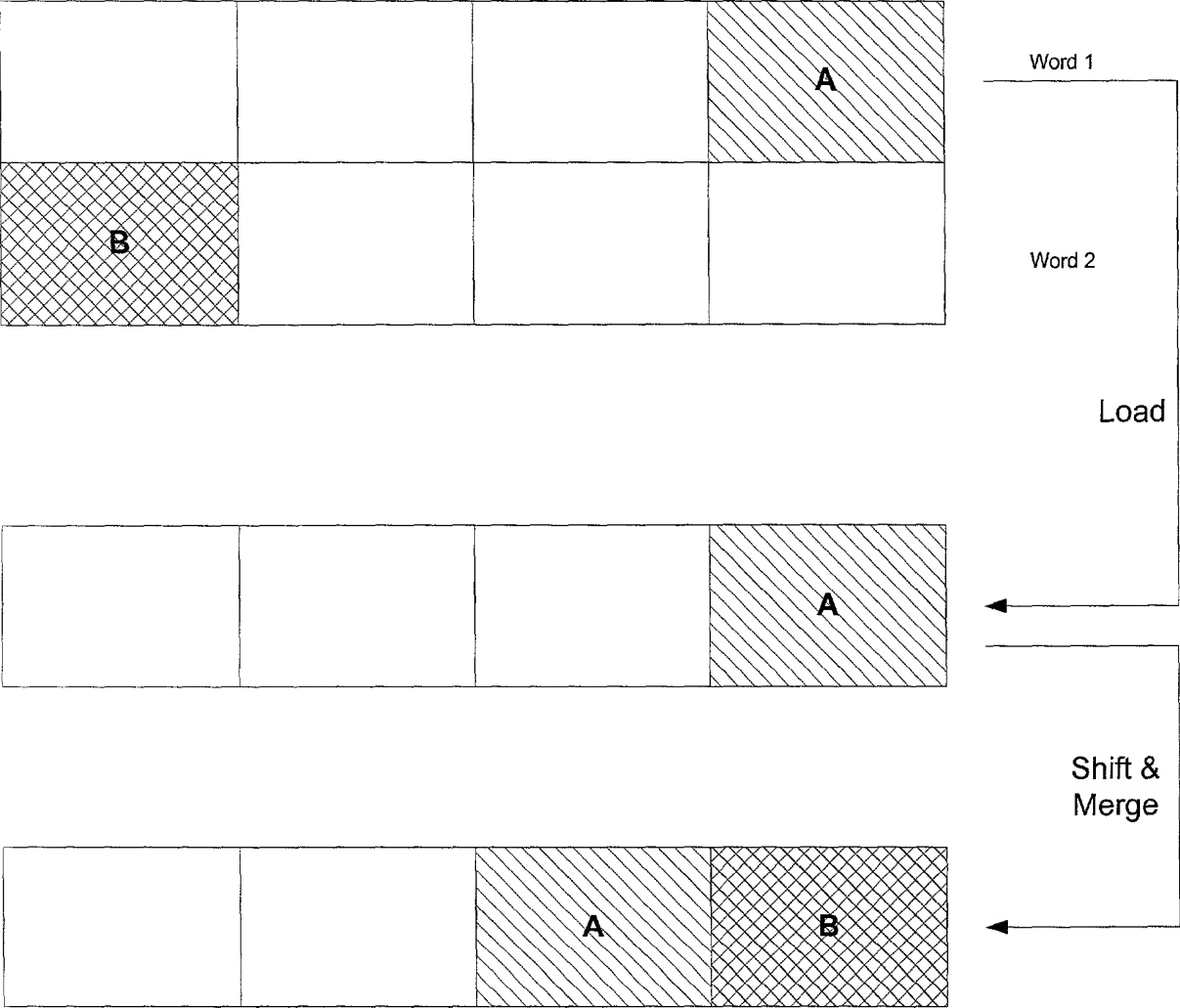


Figure 8

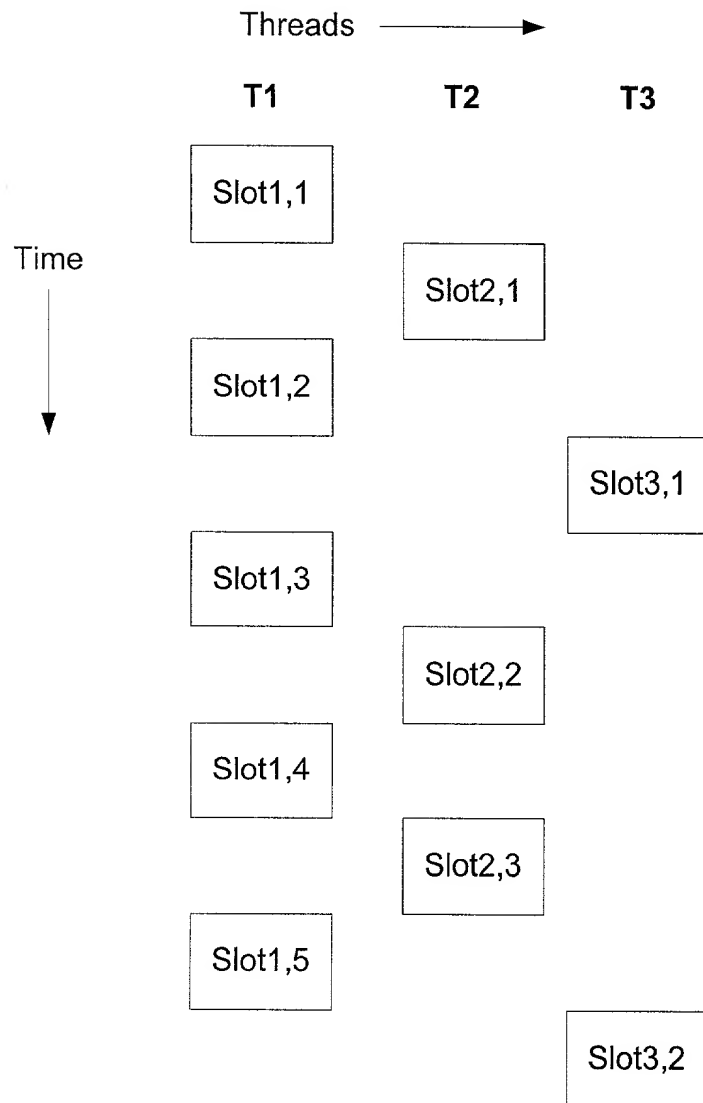


Figure 9